



PATENT

Attorney Docket No. CR0234M (72460)

2173  
#2  
SP  
8-21-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Mike Danielson et al.

Appln No.: 10/036,910

Filed: December 21, 2001

For: VIDEO SHAPE PADDING  
METHOD

Group Art  
Unit:

2173

Examiner: Unassigned

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this date.

8/14/03

Date

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INFORMATION DISCLOSURE STATEMENT

Technology Center 2100

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Pursuant to the duty of disclosure under 37 CFR § 1.56, and in accordance with 37 CFR §§ 1.97 and 1.98, Applicants bring the following information with respect to the above-identified application to the attention of the Examiner.

NON PATENT LITERATURE DOCUMENTS

Christoph HEER and Kay MIGGE; "VLSI Hardware accelerator for the MPEG-4 padding algorithm"; Part of the IS&T/SPIE Conference on Media Processors 1999, San Jose, California, January 1999; SPIE Vol. 3655; pgs. 113-119

The above document is listed on Form PTO/SB/08 which accompanies this Information Disclosure Statement, and a copy of each document listed is enclosed herewith.

Pursuant to 37 CFR § 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 CFR § 1.56(b).

Respectfully submitted,

By: 

Steven G. Parmelee  
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Date: August 14, 2003

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<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.